IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Czech et al	**GROUP:**	2826
SERIAL NO:	09/852,123	**EXAMINER:**	Johannes P. Mondt
FILED:	May 8, 2001		
FOR:	ELECTROSTATIC DISCHARGE PROTECTIVE STRUCTURE		

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

AMENDED APPEAL BRIEF

This amended appeal brief is in response to the Notification of Non-Complaint Appeal Brief dated May 8, 2006. The Evidence Appendix and Related Proceedings Appendix are now included.

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date below, with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Sarah L. Henry

5/16/06
Date

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I. REAL PARTY OF INTEREST

The real party of interest is Micronas GmbH of Freiburg, Germany.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF CLAIMS

On October 20, 2004 the appellant appealed from the final rejection of claims 1-12 under 35 U.S.C. §103. Claims 1-12, which are set forth in Appendix A attached hereto, are all the remaining claims in this application. The rejection of claims 1-12 is being appealed.

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the final rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention relates to the field of semiconductor devices, and in particular to an electrostatic discharge (ESD) protective structure to protect an integrated semiconductor circuit against electric discharge.

Claim 1 recites an electrostatic discharge (ESD) protective structure (e.g., see element 7 in FIG. 2) that protects an integrated circuit connected between a first voltage bus with a first supply voltage (e.g., VCC) and a second voltage bus with a second supply voltage (e.g., VSS). The electrostatic discharge protective structure (e.g., element 7 in FIG. 2) includes a plurality of laterally designed bipolar transistors (e.g., T1-T3 in FIG. 2) each having a first load line (e.g., C in FIG. 2) connected to the first voltage bus (e.g., element 4 in FIG. 2) and a second load line (e.g., element E in FIG. 2) connected to the second voltage bus (e.g., element 5 in FIG. 2). The first load lines (e.g., C in FIG. 2) are electrically parallel to one another, and the second load lines (e.g., E in FIG. 2) are electrically parallel to one another. Each of the laterally designed bipolar transistors (e.g., T1-T3 in FIG. 2) includes a control connection (e.g., B in FIG. 2) connected to one of the voltage buses. Significantly, a single track resistor (e.g., RB in FIG. 2) is co-integrated into a semiconductor body (e.g., element 10 in FIG. 3), where the single track resistor (e.g., RB) precedes every control connection (e.g., B) of the laterally designed bipolar transistors (T1-T3).

The various elements recited in claim 1 are discussed in the specification in at least the following locations, amongst others:

FEATURES OF CLAIM 1	SPECIFICATION
electrostatic discharge (ESD) protective structure	Pg. 7, lines 11-12, *inter alia*
a first supply voltage (e.g., VCC)	Pg. 7, line 4, *inter alia*
second supply voltage (e.g., VSS)	Pg. 7, line 4, *inter alia*
plurality of laterally designed bipolar transistors (e.g., T1-T3 in FIG. 2)	Pg. 7, lines 11-14, *inter alia*
first load line (e.g., C in FIG. 2)	Pg. 7, lines 13-14, *inter alia*
first voltage bus (e.g., element 4 in FIG. 2)	Pg. 7, lines 3-6; lines 9-10 and lines 11-13, *inter alia*
second load line (e.g., element E in FIG. 2)	Pg. 7, lines 13-14, *inter alia*
second voltage bus (e.g., element 5 in FIG. 2)	Pg. 7, lines 3-6; lines 9-10 and lines 11-13, *inter alia*
a control connection (e.g., B in FIG. 2)	Pg. 7, lines 16-19, *inter alia*
a single track resistor (e.g., RB in FIG. 2) is co-integrated into a semiconductor body (e.g., element 10 in FIG. 3),	Pg. 7, lines 16-19, *inter alia*
where the single track resistor (e.g., RB) precedes every control connection (e.g., B) of the laterally designed bipolar transistors (T1-T3).	Pg. 4, lines 8-9; Pg. 7, lines 16-19 , *inter alia*

Claim 2 recites the features of that the semiconductor body (e.g., element 10 in FIG. 3) has embedded therein at least one emitter zone (e.g., element 13 in FIG. 3) and at least one collector zone (e.g., element 12 in FIG. 3) of the first conduction type and at least one base zone (e.g., element 15 in FIG. 3) of the second, opposite conduction type. In addition, claim 2 recites the feature that a well-shaped region (e.g., element 17 in FIG. 3) is inserted into the semiconductor body (e.g., element 10 in FIG. 3) between the zones of the first conduction type (e.g., elements 12 and 13 in FIG. 3) and the base zone or the base zones (e.g., element

15 in FIG. 3), so as to extend the effective mean free path of the charge carriers to the base zone (e.g., element 15 in FIG. 3).

The various elements recited in claim 2 are discussed in the specification in at least the following locations, amongst others:

FEATURES OF CLAIM 2	SPECIFICATION
wherein said semiconductor body has embedded therein at least one emitter zone and at least one collector zone of the first conduction type and at least one base zone of the second, opposite conduction type,	Pg. 7, line 20 - Pg. 8, lines 20, *inter alia*
wherein a well-shaped region is inserted into said semiconductor body between said zones of the first conduction type and said base zone or said base zones,	Pg. 8, line 13 - Pg. 9, line 4, *inter alia*
so as to extend the effective mean free path of the charge carriers to said base zone.	Pg. 5, lines 1-2, Pg. 8, lines 21-29; Pg. 9, line 2, *inter alia*

Claim 6 recites the feature that the base zones (e.g., element 14 in FIG. 3) laterally enclose the emitter zones (e.g., element 13 in FIG. 3) and the collector zones (e.g., element 12 in FIG. 3).

The various elements recited in claim 6 are discussed in the specification in at least the following locations, amongst others:

FEATURES OF CLAIM 6	SPECIFICATION
wherein said base zones laterally enclose said emitter zones and said collector zones.	Pg. 5, lines 11-12; Pg. 8, lines 6-7, *inter alia*

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claim 1 is obvious in view of the combined subject matter disclosed in U.S. Patent 5,043,782 to Avery (hereinafter "Avery") and Japanese Patent Application JP361292351A to Wada et al (hereinafter "Wada"), in the alternative Avery in view of U.S. Patent 6,147,852 to Ravanelli (hereinafter "Ravanelli").

Whether claims 2-5 are obvious in view of the combined subject matter disclosed in Avery, Wada and U.S. Patent 6,075,271 to Smith (hereinafter "Smith").

Whether claim 6 is obvious in view of the combined subject matter disclosed in Avery, Wada, Smith and U.S. Patent 5,623,387 to Li et al (hereinafter "Li").

Whether claims 7-12 are obvious in view of the combined subject matter disclosed in Avery, Wada, Smith, Li and U.S. Patent 6,277,689 to Wong (hereinafter "Wong").

VII. ARGUMENT

CLAIM 1

Claim 1 recites an electrostatic discharge protective structure arranged to protect an integrated circuit connected between a first voltage bus having a first supply voltage (VCC) and a second voltage bus having a second supply voltage (VSS). The protective structure includes:

> "a single track resistor (RB) co-integrated into a semiconductor body, wherein said single track resistor precedes every control connection (B) of said laterally designed bipolar transistors (T1-T3)." (cl. 1)

Significantly, the protective device of claim 1 includes a single track resistor that precedes each of the control connections of the bipolar transistors.

A. A Prima Facie Case of Obviousness Has Not Been Presented

After admitting that Avery does not teach a single-track resistor to precede every control connection in order to enable a large input surge voltage to be more uniformly dispersed, the Official Action then contends that Wada teaches the application of one track resistor (see Official Action, pg. 4). The Official Action then abruptly concludes *"it would have been obvious to one of ordinary skill in the art to modify the invention by Avery at the time it was made so as to include the stipulation that a single-track resistor be included as stipulated in claim 1 of Applicants."* (Official Action, pg. 4).

"Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching suggestion or incentive supporting the combination." In re Geiger, 2 U.S.P.Q.2d 1276, 1278 (Fed. Cir. 1987). *"Although the Commissioner suggests that [the structure in the primary prior art reference] could readily be*

modified to form the [claimed] structure, '[t]he mere fact that the prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the modification.'" In re Laskowski, 10 U.S.P.Q.2d 1397, 1398 (Fed. Cir. 1989), citing In re Gordon, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984). In addition, *"[w]hen the incentive to combine the teachings of the references is not readily apparent, it is the duty of the examiner to explain why the combination of the reference teachings is proper."* Ex parte Stone, 2 U.S.P.Q.2d 1788, 1790 (Bd.App. & Int'f 1986) (emphasis added).

The Official Action is void of any proper reasoning regarding why one of ordinary skill would have modified Avery. As noted above, it is fundamental that obviousness can not be established absent some teaching to combine the references, or a suggestion or incentive supporting the combination of references. See In re Gieger, at 1278 (Fed. Cir. 1987). It is respectfully submitted that a prima facia case of obviousness has not been presented since there is no proper teaching, suggestion or incentive of record in the Official Action that would lead one of ordinary skill in the art to modify Avery as suggested. Specifically, noticeably missing from the Official Action is the necessary cite to a teaching or suggestion in the prior art references as to why someone would combine Avery and Wada in the manner suggested in the Official Action. The mere contention that two references can be combined is not sufficient to establish a prima facie case of obviousness.

B. There is no Proper Combination of References Which Disclose the Invention Set Forth in Claim 1

Assuming for the moment, without admitting, that Avery and Wada are properly combinable, then modifying Avery based upon the teaching of Wada still fails to render claim 1

obvious. As set forth above, Avery does not disclose (nor suggest) a protective device having a plurality of transistors, wherein a single track resistor precedes a control connection on each of the plurality of transistors.

Wada discloses that the channel length L of the transistor is gradually reduced to gradually decrease a breakdown voltage BVDS between the source and the drain. As a result, an input surge voltage can be uniformly dispersed in the channel of the transistor. Significantly, in Wada, the resistor 2 does not cause the current to be uniformly distributed to the protecting MIS transistors 4. Varying the channel length L for each of the transistors 4 as shown in FIG. 1 of Wada is what causes the uniform current flow.

One of ordinary skill in the art would not look to Wada, since Wada discloses varying the channel length. As set forth in Avery, a shorter channel length transistor QS is used to drive a longer channel length structure QL into conduction. If the long channel length of the transistors QL were modified to include channel lengths of various sizes, then the circuit of Avery may no longer operate for its intended purpose. Avery expressly discloses a system design that employs the shorter channel length transistor QS that is used to drive the longer length channel structure transistor QL into conduction. If the channel length of transistors QL are gradually decreased, then Avery may no longer conduct properly and snap back. Therefore, a skilled person would not modify the selected long channel lengths of Avery to include the gradual reduced channel lengths disclosed in Wada.

In addition, modifying Avery according to Wada may result in an **in**operable device.

With respect to the combination of Avery and Ravanelli, the Official Action cites to FIG. 1 and col. 1, lines 38-45 in Ravanelli and contends Ravanelli *"teaches the inclusion of one track*

resistor as Prior Art, said track resistor being co-integrated into a semiconductor body so as to precede every control connexion [sic] of a plurality of laterally designed bipolar transistors:" (Official Action, pg. 4). However, the cited section from the Background of the Invention section of Ravanelli merely states *"[f]or example, some circuits typically used to protect input terminals employ resistors in series or diodes in series or in parallel that are integrated into the substrate of the integrated circuit itself in order to limit the currents caused by ESDs".* (emphasis added, col. 1, lines 41-45). Therefore, it is respectfully submitted that the characterization in the Official Action of the cited paragraph from Ravanelli is impermissibly broad and incorrect. Specifically, the express cited language of Ravanelli clearly mentions the use of *"...resistors in series or diodes in series or in parallel..."* (col. 1, lines 42-43). Based upon this rather limited express language of Ravanelli, the contention in the Official Action regarding what Ravanelli teaches is improper, and perhaps tainted by insidious hindsight. Specifically, Ravanelli certainly does not teach *" the inclusion of one track resistor as Prior Art,"* as alleged in the Official Action. (Official Action, pg. 4). In fact, the section of Ravanelli cited in the Official Action fails to even use the singular term resistor. In addition, the cited sections of Ravanelli do not even mention laterally designed bipolar transistors, contrary to the contention on page 4, lines 12-14 of the Official Action. Accordingly, it is respectfully submitted that the mischaracterization of Ravanelli in the Official Action is based on an impermissibly broad reading of Ravanelli.

CLAIMS 2-5

Claims 2-5 currently stand rejected under 35 U.S.C. §103 for allegedly being obvious in view of the combined subject matter disclosed in Avery, Wada and U.S. Patent 6,075,271 to Smith (hereinafter "Smith").

It is respectfully submitted that this rejection is now moot, since claim 1 is patentable for at least the reasons set forth above.

It is respectfully submitted that a prima facie case of obviousness has not been presented, for at least the reasons set forth above with respect to claim 1. We shall now discuss the combination of Avery, Wada and Smith.

Claim 2 recites:

> "wherein said semiconductor body has embedded therein at least one emitter zone and at least one collector zone of the first conduction type and at least one base zone of the second, opposite conduction type, wherein a well-shaped region is inserted into said semiconductor body between said zones of the first conduction type and said base zone or said base zones, so as to extend the effective mean free path of the charge carriers to said base zone." (emphasis added, cl. 2)

It is recognized that neither Avery nor Wada teaches such a well shaped region (see the Official Action, pg. 5). It is then alleged that Smith discloses such a well and that a skilled person would have modified the subject matter disclosed in Avery and Wada to include such a well.

A fair and proper reading reveals that Smith has nothing to do with ESD protective devices. Smith simply discloses a stacked gate buffer. FIG. 1 of Smith illustrates an ESD circuit 15. However, Smith clearly states that this ESD circuit 15 is not disclosed within the specification or figures of the patent (see Smith, col. 3, lines 51-56). The deeper doped region 80 referred to in Smith has nothing to do with an ESD device. For example, FIG. 1 shows that the deeper doped region 80 is associated with the stacked buffer and not the ESD structure. Hence, it

is respectfully submitted that a skilled person working in the field of ESD devices would not combine Smith with Avery and Wada since Smith does not relate to ESD devices.

CLAIM 6

Claim 6 currently stands rejected under 35 U.S.C. §103 for allegedly being obvious in view of the combined subject matter disclosed in Avery, Wada, Smith and U.S. Patent 5,623,387 to Li et al (hereinafter "Li").

It is respectfully submitted that this rejection is now moot, since claim 1 is patentable for at least the reasons set forth above, along with claims 2-5.

In addition, it is respectfully submitted that a prima facie case of obviousness regarding claim 6 has not been presented, for at least the reasons set forth above with respect to claim 1. We shall now discuss the combination of Avery, Wada, Smith and Li.

CLAIMS 7-12

Claims 7-12 currently stand rejected under 35 U.S.C. §103 for allegedly being obvious in view of the combined subject matter disclosed in Avery, Wada, Smith, Li and U.S. Patent 6,277,689 to Wong et al (hereinafter "Wong").

It is respectfully submitted that this rejection is now moot, since claim 1, claims 2-5 and claim 6 are patentable for at least the reasons set forth above.

CONCLUSION

For all the foregoing reasons, we submit that the rejection of claims 1-12 is erroneous and reversal thereof is respectfully requested.

If there are any fees due in connection with the filing of this appeal brief, please charge them to our Deposit Account 50-3381. If a fee is required for any extension of time under 37 C.F.R. §1.136 not accounted for above, such an extension is requested and the fee should be charged to the above Deposit Account.

Respectfully submitted,

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CLAIMS APPENDIX

1.(Previously Presented) An electrostatic discharge (ESD) protective structure that protects an integrated circuit connected between a first voltage bus with a first supply voltage (VCC) and a second voltage bus with a second supply voltage (VSS), said electrostatic discharge protective structure comprising:

a plurality of laterally designed bipolar transistors each having a first load line connected to the first voltage bus and a second load line connected to the second voltage bus, wherein said first load lines are electrically parallel to one another and said second load lines are electrically parallel to one another, each of said laterally designed bipolar transistors includes a control connection connected to one of the voltage buses;

a single track resistor (RB) co-integrated into a semiconductor body, wherein said single track resistor precedes every control connection (B) of said laterally designed bipolar transistors (T1-T3).

2.(Previously Presented) The electrostatic discharge protective structure of claim 1, wherein said semiconductor body has embedded therein at least one emitter zone and at least one collector zone of the first conduction type and at least one base zone of the second, opposite conduction type, wherein a well-shaped region is inserted into said semiconductor body between said zones of the first conduction type and said base zone or said base zones, so as to extend the effective mean free path of the charge carriers to said base zone.

3.(Original) The electrostatic discharge protective structure of claim 2, wherein said well-shaped region is connected to one of said zones of the first conduction type.

4.(Original) The electrostatic discharge protective structure of claim 3, wherein said well-shaped region has the same conduction type as said zone to which it is connected, but has a lower dopant concentration.

5.(Original) The electrostatic discharge protective structure of claim 4, wherein said well-shaped region extends deeper into said semiconductor body than said zone which it adjoins or to which it is connected.

6.(Previously Presented) The electrostatic discharge protective structure of claim 5, wherein said base zones laterally enclose said emitter zones and said collector zones.

7.(Original) The electrostatic discharge protective structure of claim 6, wherein said semiconductor body has charge carriers of the first conduction type and that at least one further well of the second conduction type is embedded in said semiconductor body, and that said emitter zones, collector zones, and base zones and said well-shaped regions are embedded in said well.

8.(Original) The electrostatic discharge protective structure of claim 7, wherein said emitter zones and collector zones are designed as strips and are disposed alternatingly next to one another and parallel to one another.

9.(Original) The electrostatic discharge protective structure of claim 8, wherein said electrostatic discharge protective structure is configured and arranged in an essentially square layout.

10.(Original) The electrostatic discharge protective structure of claim 9, wherein in said emitter zones are through-contacted by said emitter electrodes, and said collector zones are through-contacted by said collector electrodes.

11.(Original) The electrostatic discharge protective structure of claim 8, wherein said emitter electrodes and said collector electrodes are connected via conductor tracks to oppositely situated voltage buses and form finger-like connections which are staggered with one another.

12.(Original) The electrostatic discharge protective structure of claim 8, wherein said bipolar transistors (T1-T3) are designed as field oxide transistors.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None